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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,053	12/20/2001	Dana L. Rose	30320/37779	2228

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/027,053	ROSE ET AL.
	Examiner	Art Unit
	Joseph D. Torres	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-22* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-4, drawn to A System for Detecting Bit Errors Comprising a multi-source agreement compliant electrical connector, wherein the multi-source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit, classified in class 714, subclass 799.

II. Claims 5-9, drawn to A System for Determining a Bit Error Rate Comprising a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream, classified in class 714, subclass 724.

III. Claims 10-12, drawn to A Printed Circuit Assembly for Use in Detecting a Bit Error Rate Comprising: a printed circuit board; a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; classified in class 714, subclass 704.

IV. Claims 13-15, drawn to An Apparatus for Testing a Multi-Source Agreement Compliant Optical Transceiver Comprising a multi-source agreement compliant electrical connector disposed on the printed circuit substrate and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; and a bit error indication circuit disposed on the printed circuit substrate; classified in class 714, subclass 742.

V. Claims 16-19, drawn to A Method of Testing an Optical Transceiver Comprising: directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device; classified in class 714, subclass 742.

VI. Claims 20-22, drawn to A method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA

compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber; classified in class 714, subclass 745.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as in a multi-source agreement compliant electrical connector, wherein the multi- source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit. In the instant case, invention Group II has separate utility such as in a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream. See MPEP § 806.05(d).

Inventions Group I and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each

other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as in a multi-source agreement compliant electrical connector, wherein the multi- source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit. In the instant case, invention Group III has separate utility such as in a printed circuit assembly for use in detecting a bit error rate comprising: a printed circuit board; a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit. See MPEP § 806.05(d).

Inventions Group I and Group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as in a multi-source agreement compliant electrical connector, wherein the multi- source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit. In the instant case, invention Group IV has separate utility such as a multi-source agreement compliant electrical connector disposed on the printed circuit substrate and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; and a bit error indication circuit disposed on the printed circuit substrate. See MPEP § 806.05(d).

Inventions Group I and Group V are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case Group V can be used for directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device.

Inventions Group I and Group VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as in a multi-source agreement compliant electrical connector, wherein the multi- source agreement compliant electrical connector is adapted to convey the transmitted and received bit streams and is in communication with the bit stream comparison unit. In the instant case, invention Group VI has separate utility such as a method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant

optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber. See MPEP § 806.05(d).

Inventions Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II has separate utility such as in a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream. In the instant case, invention Group III has separate utility such as in a printed circuit assembly for use in detecting a bit error rate comprising: a printed circuit board; a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit. See MPEP § 806.05(d).

Inventions Group II and Group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II has separate utility such as in a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream. In the instant case, invention Group IV has separate utility such as a multi-source agreement compliant electrical connector disposed on the printed circuit substrate and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; and a bit error indication circuit disposed on the printed circuit substrate. See MPEP § 806.05(d).

Inventions Group II and Group IV are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case Group V can be used for directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the

comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device.

Inventions Group II and Group VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II has separate utility such as in a processing unit coupled to the bit stream generator and the bit stream comparison unit adapted to determine the bit error rate of the device under test based on the comparison of the second bit stream to the first bit stream. In the instant case, invention Group VI has separate utility such as a method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber. See MPEP § 806.05(d).

Inventions Group III and Group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III

has separate utility such as in a printed circuit assembly for use in detecting a bit error rate comprising: a printed circuit board; a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit. In the instant case, invention Group IV has separate utility such as a multi-source agreement compliant electrical connector disposed on the printed circuit substrate and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit; and a bit error indication circuit disposed on the printed circuit substrate. See MPEP § 806.05(d).

Inventions Group III and Group V are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case Group V can be used for directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the

comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device.

Inventions Group III and Group VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility such as in a printed circuit assembly for use in detecting a bit error rate comprising: a printed circuit board; a bit stream comparison circuit disposed on the printed circuit board and adapted to generate an output for use in detecting the bit error rate; and a multi-source agreement compliant electrical connector disposed on the printed circuit board and electrically coupled to the bit stream generation circuit and the bit stream comparison circuit. In the instant case, invention Group VI has separate utility such as a method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber. See MPEP § 806.05(d).

Inventions Group IV and Group V are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case Group V can be used for directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device.

Inventions Group IV and Group VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group VI has separate utility such as a method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant

optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber. In the instant case, invention Group VI has separate utility such as a method for determining a Bit Error Rate for each of a plurality of MSA compliant Optical Receivers directly connecting each of the plurality of MSA compliant optical transceivers to a respective one of a plurality of printed circuit assemblies, each of which includes an MSA compliant connection and each of which is adapted to detect bit errors in a bit stream received from its respective one of the plurality of MSA compliant optical transceivers; placing the plurality of MSA compliant optical transceivers and the plurality of printed circuit assemblies in an environmental test chamber; and detecting bit errors associated with each of the plurality of MSA compliant optical transceivers while each of the plurality of MSA compliant optical transceivers is under test in the environmental test chamber. See MPEP § 806.05(d).

Inventions Group V and Group VI are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case can be used for directly connecting the optical transceiver to a printed circuit assembly via a multi-source agreement compliant connection; transmitting a first bit stream from the printed circuit assembly to the optical

transceiver via the multi- source agreement compliant connection; receiving a second bit stream from the optical transceiver at the printed circuit assembly via the multi-source agreement compliant connection; comparing the list and second bit streams at the printed circuit assembly; detecting a bit error of the optical transceiver based on the comparison of the first and second bit streams; and displaying an indication of the detected bit error via a display device.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search strategies required for Groups I-VI are mutually distinct, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Mark Hanley on 29 July 2004 to request an oral election to the above restriction requirement, but did not result in an election being made.

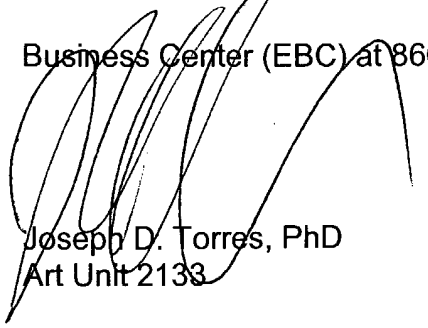
Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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